Amendments to the Specification

Delete the paragraph starting at Page 4, Line 26 and substitute therefor:

FIG. 2 illustrates a cross section of the device 100 shown in FIG. 1 showing how the parasitic SCR is formed in the P-SUBSTRATE 106 and the N-WELL region 114. The P-SUBSTRATE 106 has an internal resistance RSub and the N-WELL region 106 has an internal resistance RWell. One transistor, [Q1] Q2 is in the P-Substrate 106, and another transistor [Q2] Q1 is in the N-Well region 114. The parasitic SCR between output VOUT 110 and VCC 126 can be seen to be formed *via* p implant/deposition region 112, n-well region 114, p implant/deposition region 116, and n+ implant/deposition region 118 (PNPN). The parasitic SCR can conduct current equally well in both directions. The parasitic SCR between VOUT 110 and VSS 128 can be seen to be formed *via* n implant/deposition region 120, p-substrate region 106, n implant/deposition region 122, and p+ implant/deposition 124 (NPNP).

Delete the paragraph starting at Page 5, Line 21 and substitute therefor:

Device [400] 300 has a parasitic SCR that has its anode tied to the I/O PAD 304 and not directly to VDD. Current can flow from the I/O PAD 304 to GND through the parasitic SCR if the voltage at the I/O PAD 304 is higher than the holding voltage of the parasitic SCR. A stress condition sufficient to activate the parasitic SCR and induce a latch-up condition may be triggered by an adjacent I/O cell, or noise, among other things. Induced latch-up caused by a parasitic PNPN structure, for example, associated with the second ESD protection circuit as a consequence of stress applied on an another (*e.g.* the first) ESD protection circuit may cause the second ESD protection circuit to sink a high amount of current from its associated I/O PAD 304 connection.

Delete the paragraph starting at Page 6, Line 24 substitute therefor:

FIG. 4 illustrates a system 400 in accordance with an aspect of the present invention. The system 400 can test an integrated circuit (IC) 402 for induced latch-up and detect low impedance paths that could not be discovered using conventional testing techniques. The IC 402 has input pins 406 and output pins 408. The number of input and output pins can vary from at least one, to any number greater than one. Power from a power supply 410 is supplied to a power supply input (VCC) [418] 420 and to input pins 406. For testing, the power supply 410 can be set at the maximum allowable level for the IC 402. The output pins 408 remain unconnected during the test. A first current measuring device 412 measures current from the power supply 410 to the inputs 406. A second current measuring device 414 measures current to the power supply input 418. Alternatively, a single current measuring device (not shown) can also be used. A trigger pulse over-voltage source 404 sends a voltage pulse to testing pin 416. The voltage pulse can have the maximum amplitude and pulse width allowed by the specification [for] for IC 402. Induced latch-up is detected by monitoring current measuring devices 412 and 414. The current is measured before the application of the voltage pulse, and again after the pulse is applied to test pin 416. If the measured current increased by a certain amount after the voltage pulse is applied (*e.g.*, by 3 mA or more), then an induced latch-up has occurred, indicating IC 402 has a low impedance path. If an induced latch-up occurs, a redesign of the circuit may be in order.